Floating-Point Number Divider IP Core

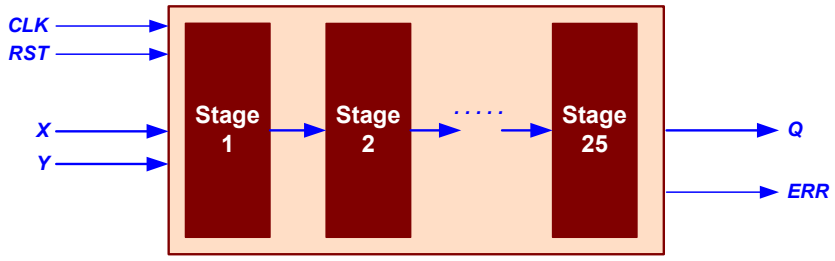
General information

The Core is intended for two floating-point 32-bit numbers dividing, which are presented in the IEEE 754 standard. High performance of the Core is achieved because of its pipelined structure. The Core could be used as a part of SoC.

Features

- *Input data word size - 32 bits (IEEE 754 standard);*
- *Output data word size – 32 bits (IEEE 754 standard);*
- *Pipelined structure, 25 pipeline stages;*
- *Input and output registers;*
- *Vendor independent VHDL model, netlist for target device.*

Floating-Point Number Divider IP Core pinout



Interface description

Pin	Activity	Description
CLK	Positive clock edge	Clock
RST	HIGH	Asynchronous Reset
X [32 - 0]	-	Input
Y [32 - 0]	-	Input
Q [32 - 0]	-	Output
ERR	HIGH	Exponent overflow flag

Sample implementation

Device	Speed grade	Utilization	Clock rate	Performance	Synthesis and implementation tools	Availability
XILINX 4000-SERIES DEVICE						
XC4036XLA-BG325	-07	898 CLB	80 MHz	2560 Mbits/s	Synplify, Xilinx	***Now***, ver_1_2_1
XILINX VIRTEX DEVICE						
XCV800-BG432	-04	1389 SLICEs	85 MHz	2770 Mbits/s	Synplify, Xilinx	***Now***, ver_1_2_2

Synplify – Synplicity Synplify VHDL Compiler, version 5.1.1;
Xilinx – Xilinx Foundation, version 2.1i (SP3).

Delivery

- Synthesizable RTL Source Codes (VHDL);
- Technology-dependent compiled netlist for the target device;
- Post-synthesis and timing models (SDF, VHD files);
- Test bench, test vectors and patterns;
- User Guide and Application Notes.

License and Price

Our HDL Source License Delivery for FPD_IEEE754 ver_1_2_x allows unlimited duplication for single product and it costs $200.

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