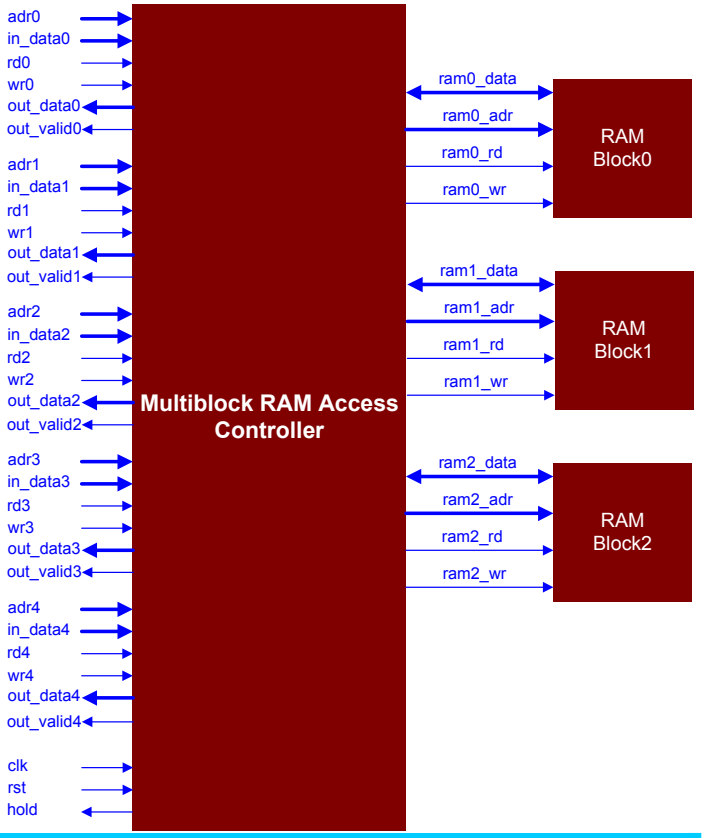
Multiple-Block RAM Access Controller IP Core

Features

- *Input address bus width – 16bit;*
- *Data bus width – 8bit;*
- *Input request lines number – 5;*
- *External RAM blocks number – 3;*
- *Fixed requests processing time – 6 clock cycles;*
- *Supported RAM size – 16kx8bit;*
- *Requests are processed in order for each requester;*
- *Improves a memory bandwidth;*
- *Vendor independent synthesizable VHDL model, netlist for target device.*

IP Core pinout



General information

Modern System-on-Chip (SoC) applications such as HDTV, DVD, Shared Memory Multiprocessor systems, become increasingly limited because of insufficient memory performance. The motivation for shared memory subsystems for SoC leads to savings of area, cost, power and development time. Conventional solution typically uses fixed bus arbitration. The RAM controller executes the requests in the order they arrive from the bus. This prevents the RAM controller from rearranging requests to optimize the performance. The performance is limited by bus-to-memory bandwidth in such system. Giving each initiator its own port of the RAM controller can increase the performance. In such case controller can optimize the performance of the RAM subsystem by reordering requests, but total memory performance is limited by memory bandwidth. In order to maximize memory bandwidth independent RAM modules must be used. Intron's Multiblock RAM Access Controller provides a complete memory system for SoC. It connects N=5 requesters to M=3 RAM blocks (16k x 8bits). Each of input requests has an information about RAM block number, address in such block, type of request (read or write) and input data (if request type is write). Controller normally serves all requests during fixed time every clock cycle. Controller overflows when the number of input requests exceeds feasible RAM blocks bandwidth. Numbers of overflow cycles depend on input requests intensity. Experimental result shows, that proposed Controller is more efficient than a Simple Controller. For example, if request intensity is 50%, than the proposed Controller bandwidth is 38% better than bandwidth of the Simple Controller. Our approach allows designing a Controller with different parameters and for different type of external RAM controllers (SRAM, DRAM, etc). The proposed Controller can be used not only as a component for SoC design but for Multiport ASIC RAM design as well.

Sample implementation

Device	Speed grade	Utilization	Clock rate	Synthesis and implementation tools	Availability
ALTERA					
EPF10K100E	-1	3090 LCs	70.92 MHz	Synplify, Max+Plus II	***Now***, ver_1_1_1

Max+PlusII – Altera Max+PlusII, version 10.1; ***Synplify*** – Synplicity Synplify Pro VHDL Compiler, version 7.0.1.

http://www.intron-innovations.com
info@intron-innovations.com